REMARKS

Claims 1-20 are all the claims pending in the application. Claim 19 is amended solely for purposes of correcting an informality. The amendment of claim 19 should therefore not present any new issues which would require further search or consideration. Entry and consideration of the present Amendment is respectfully requested.

Initially, Applicant thanks the Examiner for acknowledging the claim for foreign priority and receipt of the priority document and for indicating that the drawings filed March 24, 2004 have been accepted.

To summarize the Office Action, the specification has been objected to for informalities, claims 1-2, 8-12 and 19-20 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Knapp et al. (U.S. Patent No. 6,862,676, hereinafter "Knapp") in view of Suzuki (U.S. Patent No. 6,240,524), and claims 4 and 15 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Knapp in view of Suzuki and Lee et al. (U.S. Patent No. 6,629,271, hereinafter "Lee").

Further, the Examiner has objected to claims 3, 5-7, 13-14, and 16-18 as being dependent from a rejected base claim, but indicates that these claims would be allowable if rewritten in independent form to include all the limitations of the respective base claims and any intervening claims.

The outstanding objection and rejections are traversed, as discussed below.

Objection to the Specification

The Examiner has objected to the specification and suggests that page 3, line 14 of the specification should be amended to change "vector resistor" to --vector register--. Applicant has amended the specification in accordance with the Examiner's suggestion and requests that the objection be withdrawn.

Claim Rejections - 35 U.S.C. § 103

As noted above, claims 1-2, 8-12 and 19-20 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Knapp in view of Suzuki. Applicant respectfully traverses and submits that the rejection of these claims is improper because the Examiner has not established *prima facie* obviousness, as evidenced below.

Initially, Applicant submits that neither Knapp nor Suzuki, whether taken alone or in combination, reasonably teaches or suggests all the features of claim 1. For instance, claim 1 defines a vector information processing apparatus comprising, *inter alia*, a CPU comprising a plurality of asynchronously operating units, a main memory for storing data, and a main memory controller for controlling the writing of data in said main memory. The main memory controller, as defined by claim 1, includes a vector scatter (VSC) address buffer that holds a storage address in said main memory for each element designated by a vector scatter instruction.

As further recited, the main memory controller inhibits the outputting of a writing permission signal that permits writing to said main memory if a writing request instructs storage of the element at an identical storage address as at least one other element and the writing

request has not been processed in accordance with a sequence of element numbers defined by the vector scatter instruction. Claim 1 defines the writing permission signal as being generated according to a writing request that requests writing of an element having a smaller element number than at least one other element designated by the vector scatter instruction. Claim 1 additionally recites the feature of writing requests for writing the element and the at least one other element to the storage address in the main memory are issued respectively from the asynchronously operating units of the CPU according to the vector scatter instruction.

Contrary to the Examiner's contention, Knapp neither suggests a vector information processing apparatus, nor does Knapp suggest *at least* the features of a vector scatter address buffer holding a storage address for plural elements designated by a ***vector scatter instruction*** and a memory controller that inhibits the outputting of a writing permission signal generated according to the writing request, as claimed, which requests writing of an element having a smaller element number than at least one other element designated by the vector scatter instruction.

In this regard, Applicant notes that Knapp teaches a superscalar processor for performing out of order processing on instruction sets. *See* Knapp at col. 3, lines 22-27. Knapp proposes that a plurality of process units in the superscalar process unit operate asynchronously to avoid a process waiting state and to perform out of order processing on in-flight instructions in which dependencies between currently fetched instructions of an instruction set and previous in-flight instructions is determined and used to generate a dependency matrix for all in-flight instructions.

In contrast to a super-scalar type processor as taught by Knapp, a ***vector***-type processor processes two or more data (i.e., vector data) by one command (i.e., vector instruction). Therefore, only the dependency of two or more vector data is usually checked in a vector-type processor. Knapp's teaching of dependencies among plural instruction sets is therefore not applicable to a vector processor. Further, in the vector information processing apparatus defined by claim 1, two or more processors operate asynchronously by one vector scatter instruction. Thus, correspondence between the instruction and data are checked in every operation by controlling the correspondence between the instruction and data in the vector-type processor. As further defined by claim 1, the outputting of the writing permission signal for elements designated by the vector scatter instruction may be inhibited.

The superscalar processor of Knapp simply does not suggest a ***vector scatter instruction***, or the features of the main memory controller regarding processing of ***vector instructions***, as claimed. Indeed, in the Office Action, the Examiner apparently identifies col. 6, lines 5-18 of Knapp with respect to the vector scatter instruction processing. However, this passage merely describes determining intra-dependencies between in flight instructions so as to perform out of order processing in the superscalar processor, as noted above, in which *intra*-dependencies between instructions I(0)-I(7) in bundle 45, and *inter*-dependencies between bundle 45 and the in-flight instructions are determined so that out of order processing can be performed.

The determination of dependencies in the super scalar processor does not suggest a vector scatter instruction of a vector information processing apparatus, as defined by claim 1, nor does Knapp suggest inhibiting the output of a writing permission signal based on the processing of

element number of elements designated by a vector scatter instruction to inhibit writing of data in the ***main memory***, as claimed. Nowhere does Knapp teach any comparison of element numbers of vector data and Knapp does not suggest inhibiting the outputting of the writing permission signal which avoids a "write-write" hazard in the main memory of the vector information processing apparatus. At least for the foregoing reasons, Knapp cannot properly be relied upon to teach the features of claim 1 discussed above. Nor has the Examiner provided any rationale to suggest that Knapp's out of order processing of instructions in a super-*scalar* processor could modified so as to be applied to processing *vector* data.

Further, Applicant submits that Suzuki fails to compensate for the deficiencies of Knapp. In rejecting claim 1, the Examiner alleges that Suzuki teaches multiple operating units operating in an asynchronous manner. *See* Office Action at page 4. However, Applicant notes that Fig. 11 of Suzuki, which the Examiner refers to, also refers to a *superscalar* processor, and therefore does not suggest the features of the vector information processing apparatus of claim 1 that are deficient in Knapp for the above noted reasons.

Therefore, even assuming one of ordinary skill in the art would have been motivated to combine the teachings of Knapp and Suzuki, the combination would not teach all the features of claim 1. Accordingly, the rejection of claim 1 is improper because the Examiner has failed to establish *prima facie* obviousness. Reconsideration and withdrawal of the rejection is therefore requested.

Claim 11 defines a method of controlling a memory of a vector information processing apparatus which recites features analogous to those discussed above that are neither taught nor

suggested by Knapp in view of Suzuki. Thus, the rejection of claim 11 is improper for similar reasons. Reconsideration and withdrawal of the rejection of claim 11 is likewise requested.

With respect to dependent claims 2-10 and 12-20, Applicant submits that these claims are allowable at least by virtue of depending from claims 1 and 11, respectively, and by virtue of the features recited therein.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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